In Th Claims:

Please amend the claims as set forth below:

--66. A solid state device comprising:

a solid state material substrate having a top surface; and

a solid state material layer no more than 10 Angstroms thick and positioned on the top surface of the substrate;

at least a portion of the solid state material layer being metallurgically bonded to at least a selected portion of the [solid state device] top surface of the solid material state substrate.

67. A solid state device as in claim 66 in which the solid state material layer has at least two of the following features: a) having an atomically smoothed bottom surface; b) having a curved top surface; c) having an atomically liquid-smoothed gate bottom layer; d) made of purified material; e) made of strengthened material; f) accurate to one atomic layer in thickness; g) aged by liquid diffusion; i) fine-grained or subgrained; j) oriented grains or subgrains; k) narrow grains or subgrains; and l) stronger than unbonded material.

C1 Cont'd

68. The device as in claim 66 in which the solid state material layer has a central portion of zero bottom width which is symmetrical with respect to a central vertical bisecting plane thereof.

69. The device as in claim 66 in which the solid state material layer has an accuracy of better than several atoms on a layer dimension selected from the group consisting of thickness, depth, curvature, shape, size, chemical composition profiling, and lateral location.

70. The device as in claim 66 in which at least a portion of the solid state material layer contains solid reinforcements, whereby the bonded material layer is stronger than the unbonded solid state material itself.

71. The device as in claim 66 in which the solid state material layer is sufficiently thin and flexible so as to yield under stress preventing device failure.

72. The device as in claim 66 in which the solid state material layer is liquid-diffusion aged.

73. The device as in claim 66 having a thickness of less than a micron thereby forming a thin-film integrated circuit device.

C1 Cont'd

74. The device as in claim 66 wherein the solid state material layer has a curved major surface with a radius of curvature of less than 1 micron.

75. The device as in claim 66 in which material of the solid state material layer is purified by a melting and solidification process;

the purity of material of the solid state material layer being improved [due to the melting and solidification] by at least one order of magnitude relative to the solid state material prior to said metallurgically bonding.

76. The device as in claim 66 in which the solid state material layer has an accuracy in thickness of one atomic layer.

77. The device as in claim 66 in which the solid state material layer comprises an ion implanted region with a depth accurate to several atomic layers .

78. A solid state device as in claim 66 including:

first and second solid state material pockets positioned adjacent to each other, but laterally separated by a gap, on the top surface of the substrate;

the solid state material layer filling and bridging the gap between the two adjacent solid state material pockets; and

at least a portion of the solid state material layer having an accuracy in thickness of [no more] better than three atomic layers.

79. A solid state device as in claim 78 in which:

at least a part of the substrate is a semiconductor of a first conductivity type; and

at least one of the semiconductor pockets is of a second conductivity type forming at least one PN junction region where the part of the substrate contacts the at least one semiconductor material pocket.

C1 Cont'd

80. The device as in claim 66 in which the solid state material layer is selected from the group consisting of a gate layer and a field layer.

81. The device as in claim 66 in which the substrate material is selected from the group consisting of Si, Ge, Si-Ge, InP, InSb, GaAs, SiC, InAs, superconductor, diamond, semiconductor material, intrinsic semiconductor material, substantially electrically insulating material, and substantially electrically conducting material, and mixture thereof.

82. The device as in claim 66 selected from the group consisting of metal-oxide-semiconductor (MOS) device, conductor-insulator-semiconductor (CIS) device, thin-film integrated circuit, and flexible integrated circuit.

83. The device as in claim 78 in which:

the first and second solid state material pockets are respectively source and drain semiconductor pockets in a CMOS device and separated by a gap from each other; the solid state material layer is a gate layer filling and bridging the gap between the two pockets; and

the gate layer material has an atomically smooth surface at least on one of the top and major bottom surfaces thereof.

84. The device as in claim 83 in which each of a major portion of the substrate, solid state material pockets, and solid state material layer consists essentially of a single doped and less doped intrinsic semiconductor material whereby the device is made resistant to dynamic forces due to impacts, vibrations, and large and rapid accelerations and decelerations.

C1 cont'd

85. The device as in claim 66 including a PN junction region having a curved adjoining surface contacting the substrate to thereby reduce but not eliminate at least one of inevitable thermal mismatch stress and in situ volume change strain generated during device processing;

the remaining residual strain and stress on the curved adjoining surface of the PN junction region improving a selected device performance.

86. The device as in claim 79 in which:

the at least one PN junction region has a curved adjoining surface and;

the at least one of the first and the second solid state material pockets meets the curved adjoining portion of the at least one PN junction region.

87. The device as in claim 66 in which the solid state material layer has a shallow, highly activated doped region having much greater dopant concentrations than the thermal equilibrium phase-diagram values.

88. The device as in claim 66 in which the solid state material layer is an electrically insulating, wavy and curved field layer containing an ion-implanted [a] substance selected from the group consisting of oxygen and nitrogen.

89. The device as in claim 78 in which:

the first and second solid state material pockets are respectively source and drain semiconductor pockets in a CMOS device;

the solid state material layer is a gate layer; and

including a conductive gate electrode of an electrically conducting material to control flow of electronic carriers from the source to the drain.

90. The device as in claim 89 in which:

the gate layer material is atomically smoothed on at least one of top and bottom major surfaces thereof to achieve maximum smoothness; and

material of the gate layer being most purified at a bottom surface facing the substrate.

91. The solid state device as in claim 66 in which:

the solid state material layer is a field layer separating and electrically isolating device components from each other;

the field layer on a horizontal cross-section thereof has a plurality of curved sections; and

each curved section has an arc length defined by: $l = r \times A$ where l is the arc length, r is the radius of curvature of the arc, and A is the subtended arc angle;

each arc section being capable of flexing whereby the arc length is changed by $\text{delta } l = r \times \text{delta } A + A \times \text{delta } r$; and

the changes in delta l, delta r, and delta A all being in directions to reduce thermal mismatch strain and automatically stopping when the residual thermal mismatch strain is reduced by the changing arc length to a point such that the multiply curved field layer can tolerate without failure the residual thermal mismatch strain.

92. The solid state device as in claim 66 in which the solid state material layer is curved to minimize thermal mismatch stresses.

93. A mass-produced solid state device comprising:

a solid state material substrate;

at least one first solid state material pocket positioned on a first selected surface of the substrate; and

a solid state material layer having at least one atomically smooth major surface which contacts and metallurgically bonds the first selected surface of the substrate to a first specified portion of the at least one first solid state material pocket.

94. A solid state device as in claim 93 further comprising:

a second solid state material pocket positioned on a second selected surface of the substrate, and laterally adjacent to, but separated by a gap from, the at least one first solid state material pocket; and in which:

the solid state material layer fills the gap between the two material pockets while contacts and metallurgically bonds with a second specified portion of the second solid state material pocket.

95. A mass-produced solid state device comprising:

a solid state material substrate;

a left and a right adjacent solid state material pockets laterally separated by a gap and positioned on a common top surface of the substrate;

a curved solid state material layer which: a) [has a radius of curvature of no more than 1.0 micron] is less than 40 angstroms ; and b) is positioned on the top surface of the substrate to bridge the gap between the two solid state material pocket[; and

at least a portion of the solid state material layer being metallurgically continuously bonded to at least a selected area of the top surface of the substrate with a mechanically perfect bonding interfacial region to avoid imperfectly bonded material layer leading to poor device yield, performance, reproducibility, reliability, and life].